Single Event Effects Testing of the Intel Pentium III (P3) Microprocessor

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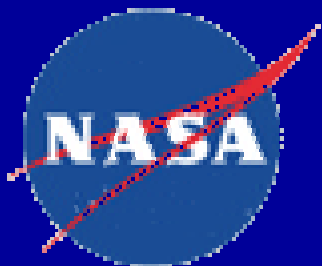**Ronald Stattel**
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Outline

- **Introduction**
- **Test Methodologies**
- **Hardware**
- **Software**
- **Test Issues**
- **Sample Data**
- **Summary**

Test Methodologies

- Single Event Effects
  - Architecture and technology implications
    - Test SOTA technology and exercise that technology
    - Exercise independent pieces of the architecture with maximum duty cycle
    - Investigate technology versus operational conditions (e.g., rated versus operation clock speeds)
  - System level impacts
    - Destructive events
    - Function interrupts vs. non-recoverable upsets vs. recoverable upsets

P3 Test Controller System
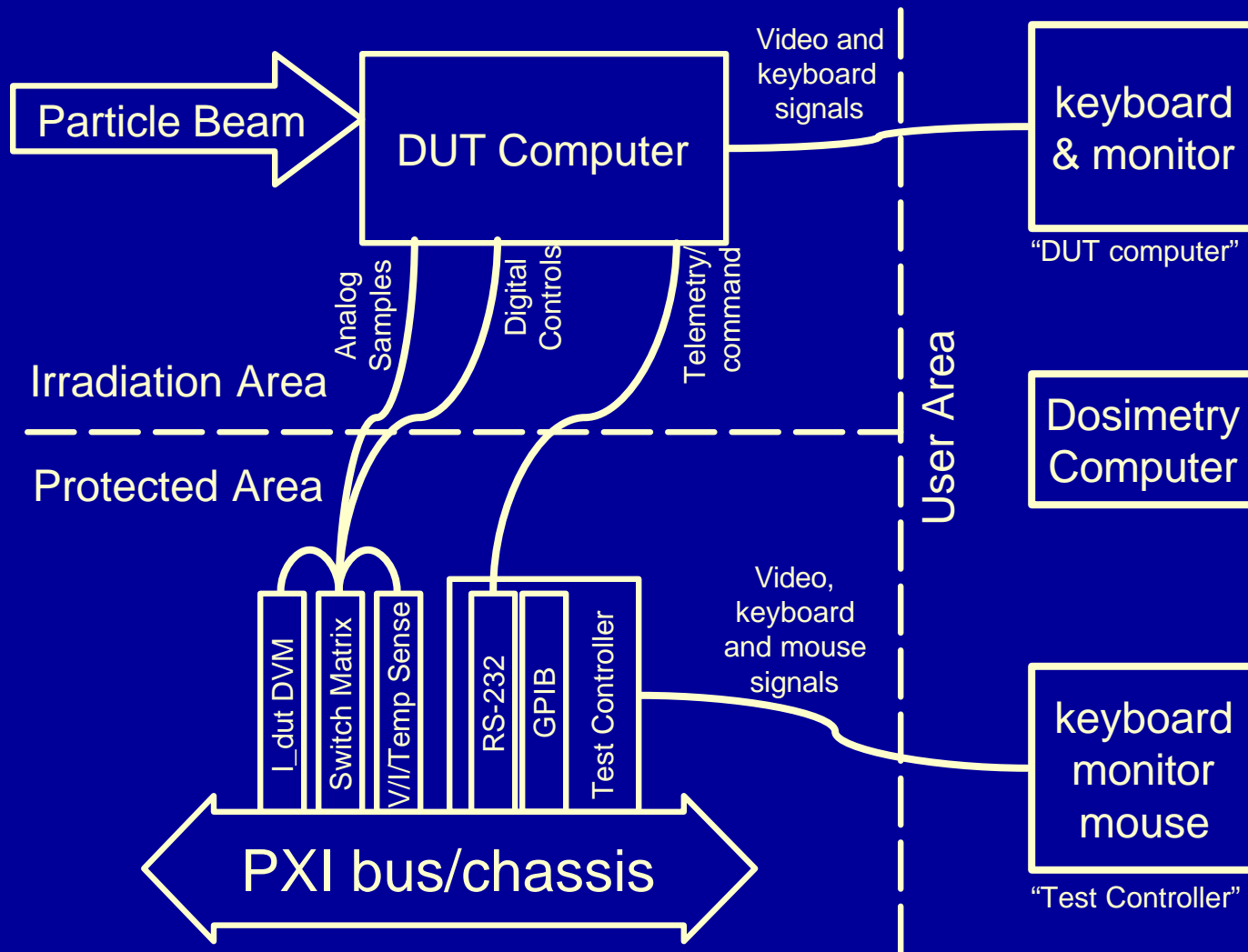
P3 DUT Computer Test System
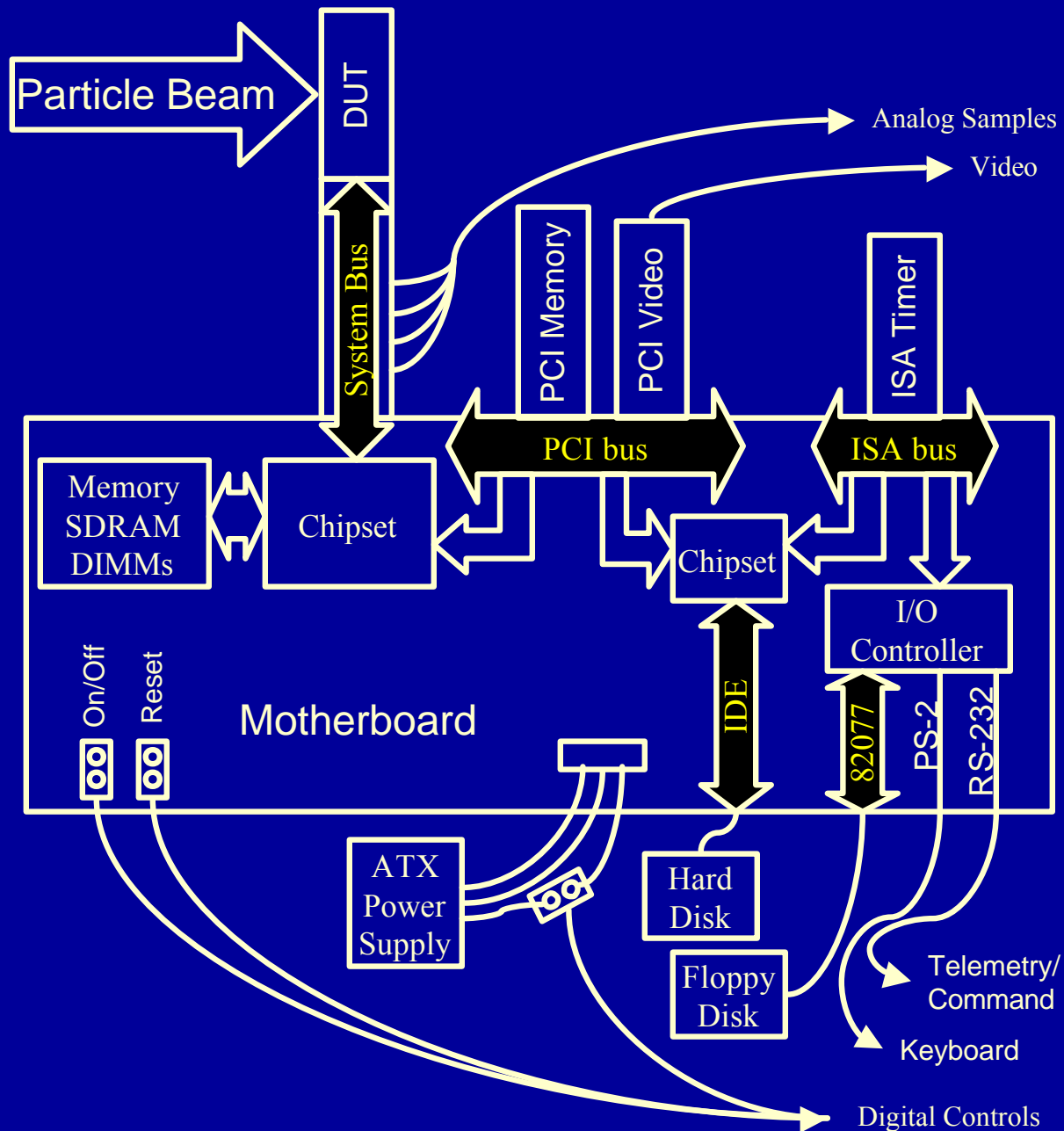
Programming Environment

- The DUT Software is written in the Microsoft Visual C++ environment with a Pharlap Add-in.

- Tests are written in a combination of C and Assembly Language.

- The software is executed on the DUT using the Pharlap Real-Time Operating System.

  - Pharlap was chosen for its low overhead, preemptive multithreading, short interrupt latency, and price.

  - The kernel has been stripped to its minimal functionality so that boot time is minimized.

  - Kernel interrupts have been disabled to allow the test running full attention of the processor.

DUT Tests

There are eight tests designed to exercise the various aspects of the CPU during SEE testing:

A: Register Test

B: Floating Point Unit Test

C: Memory/Data Cache Test - Sequential

D: Task Switching Test

E: Instruction Cache Test

F: Floating Point Unit Test (Operation Intensive)

G: MMX Test

I: Memory/Data Cache Test - Offset

Data Analysis Software

- GUI Interface

- Relational Database (3 Stages)

  - Setup data entered into database

    - Test configurations, software, dosimetry, etc.

  - Telemetry files analyzed and errors entered into database

    - Filter for allowed errors

    - Accuracy (Program shows possible errors and description)

  - SQL statements for filters to extract data

Testing Issues

- Die Penetration
  - The Pentium III die is a flip chip solder bubble bonded die.
  - The sensitive regions of the processor are approximately 900 microns deep in the silicon die.
  - Thermal issues compound Heavy Ion Testing by requiring cooling material in the beam line, as well.

- Thermal
  - The Pentium III can draw in excess of 20 watts of power.
  - The packaged heat sink and cooling fan are removed and replaced with a water-cooled jacket, that is thinned to 10 mils over the die.
  - The large thermal issue is also the reason that the die cannot be thinned.
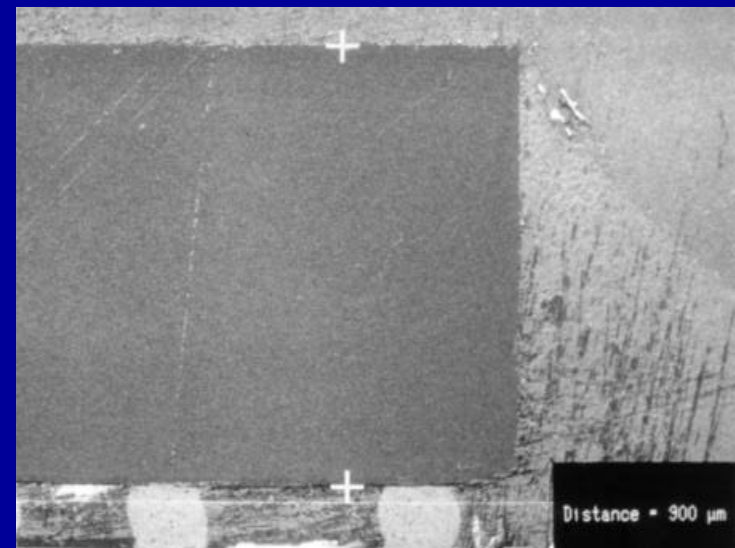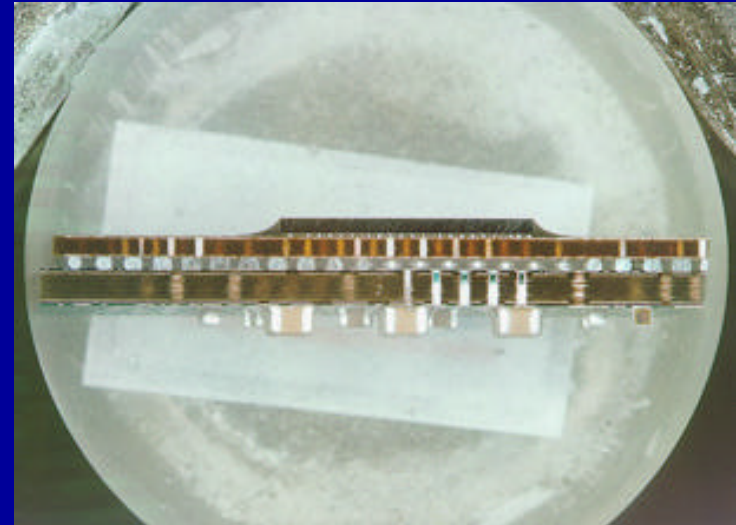
What Have We Tested

- Intel Pentium III
  - Speed ranging from 550 through 1200 MHz
  - Represents 0.25, 0.18 and 0.13 μm technology
- AMD K7
  - Speeds ranging from 600 through 1000 MHz
  - Details of technology not available
  - High SEFI rates forced the removal of these parts from the study

Where Have We Tested

- GSFC TID Facility
  - Biased and Unbiased Co-60 Testing
- Indiana University Cyclotron Facility
  - Proton Displacement Damage
  - Proton SEE
- Texas A&M University Cyclotron
  - 55 MeV/amu Argon and Neon
 - LET range from approximately 3 through 15 MeV-cm^2/mg

# TID/DDD Data

Pentium III DEVICE UNDER TEST (DUT) TABLE

Device	Rated Speed	Test Condition	Source	Exposure Levels (krads)
P3	800 MHz	Biased	Co-60	*511
P3	933 MHz	Biased	Co-60	573
P3	550 MHz	Unbiased	Co-60	336
P3	650 MHz	Unbiased	Co-60	336
P3	650 MHz	Unbiased	Co-60	3700
P3	700 MHz	Unbiased	Co-60	336
P3	850 MHz	Unbiased	Co-60	697
P3	933 MHz	Unbiased	Co-60	2100

* Indicates part functionally failed

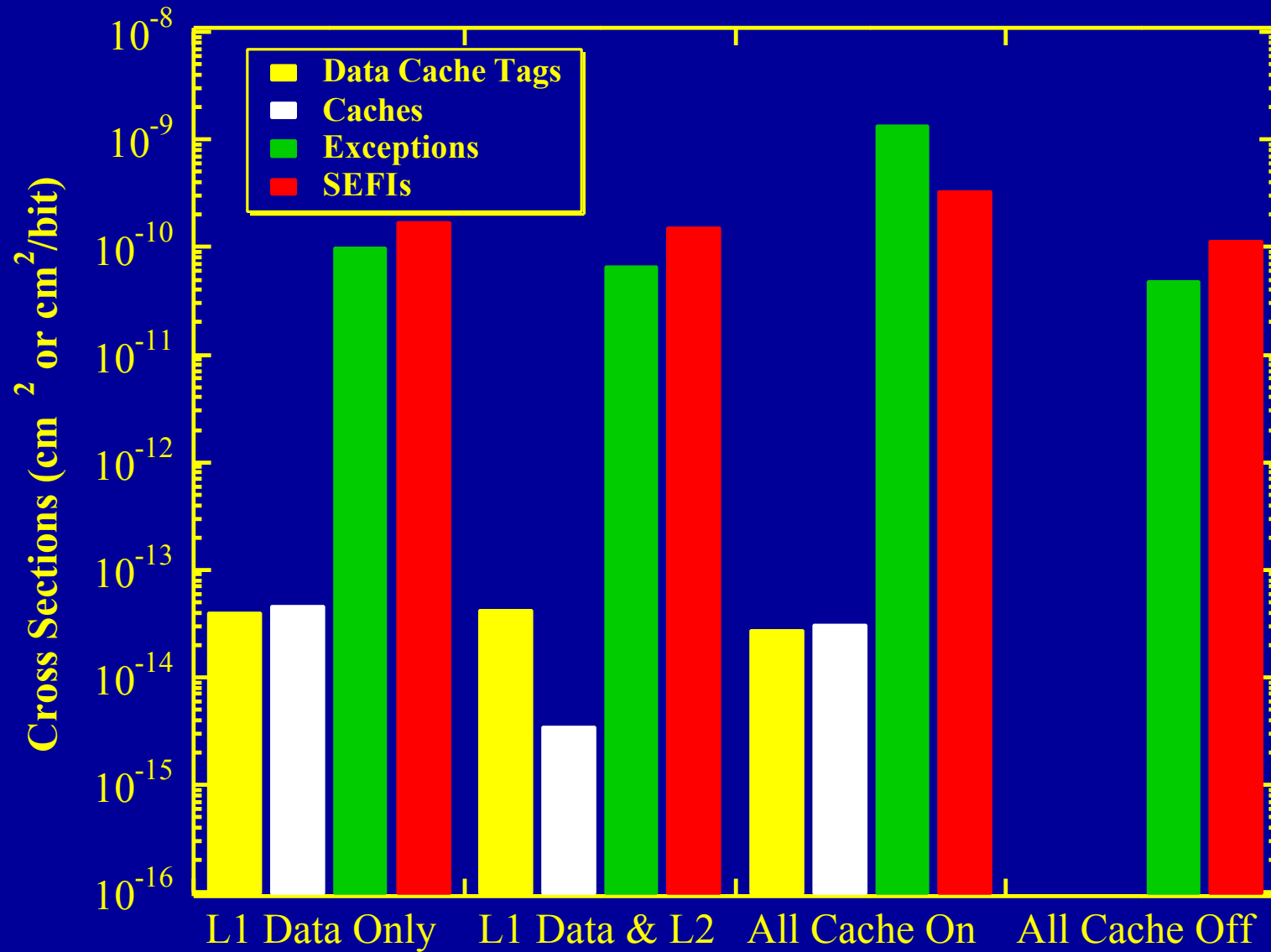# Proton SEFI Data
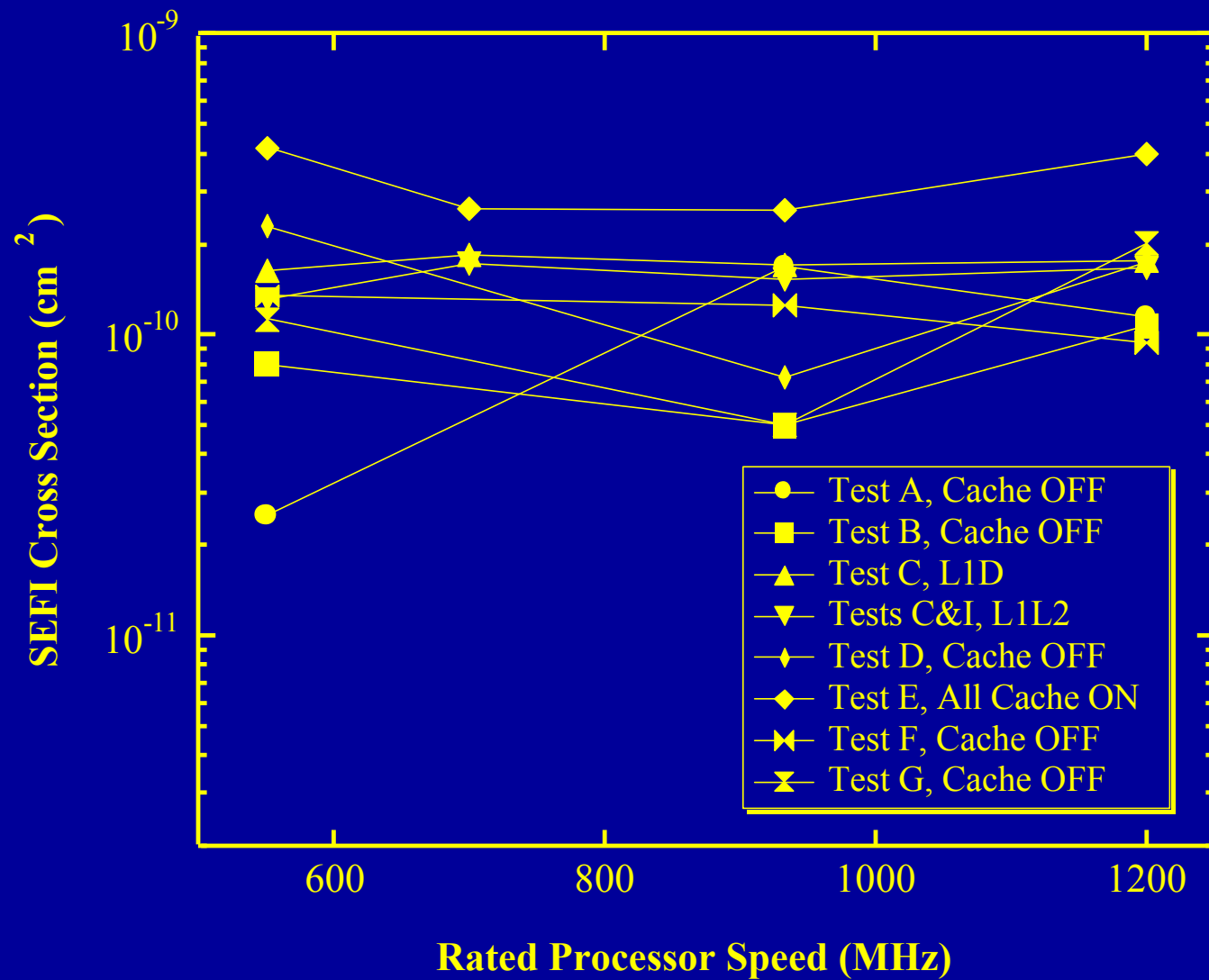
Proton L2 Cache Data
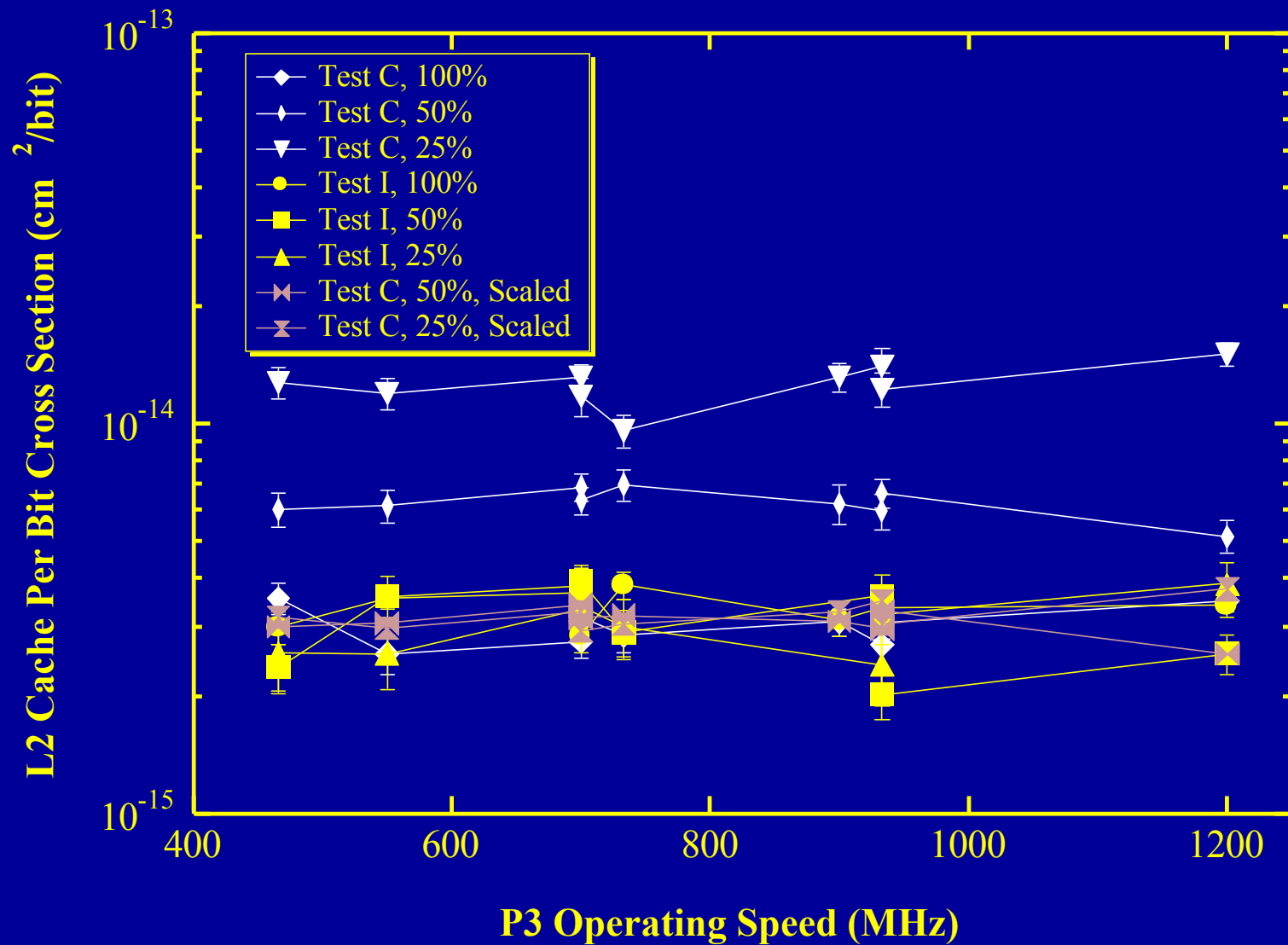
Proton Cache SEU Data

Summary Per Bit Cache Cross Sections						
Cache State	Single Tag Errors	Single TE Error	Multiple Tag Errors	Multiple TE Error	Cache Bit Errors	Cache BE Error
L1 Data	4.62×10^{-14}	2.23×10^{-14}	9.55×10^{-16}	4.78×10^{-16}	4.96×10^{-14}	7.16×10^{-15}
L2	5.72×10^{-14}	6.15×10^{-15}	1.08×10^{-15}	1.08×10^{-15}	9.86×10^{-17}	4.30×10^{-16}
L1 Inst.*	2.77×10^{-14}	4.09×10^{-15}	6.03×10^{-16}	6.03×10^{-16}	3.19×10^{-14}	1.77×10^{-15}

*Calculated values based on percentage of tag versus cache bits.*

Proton Other SEU Data

Total Cross Sections for Other Tests

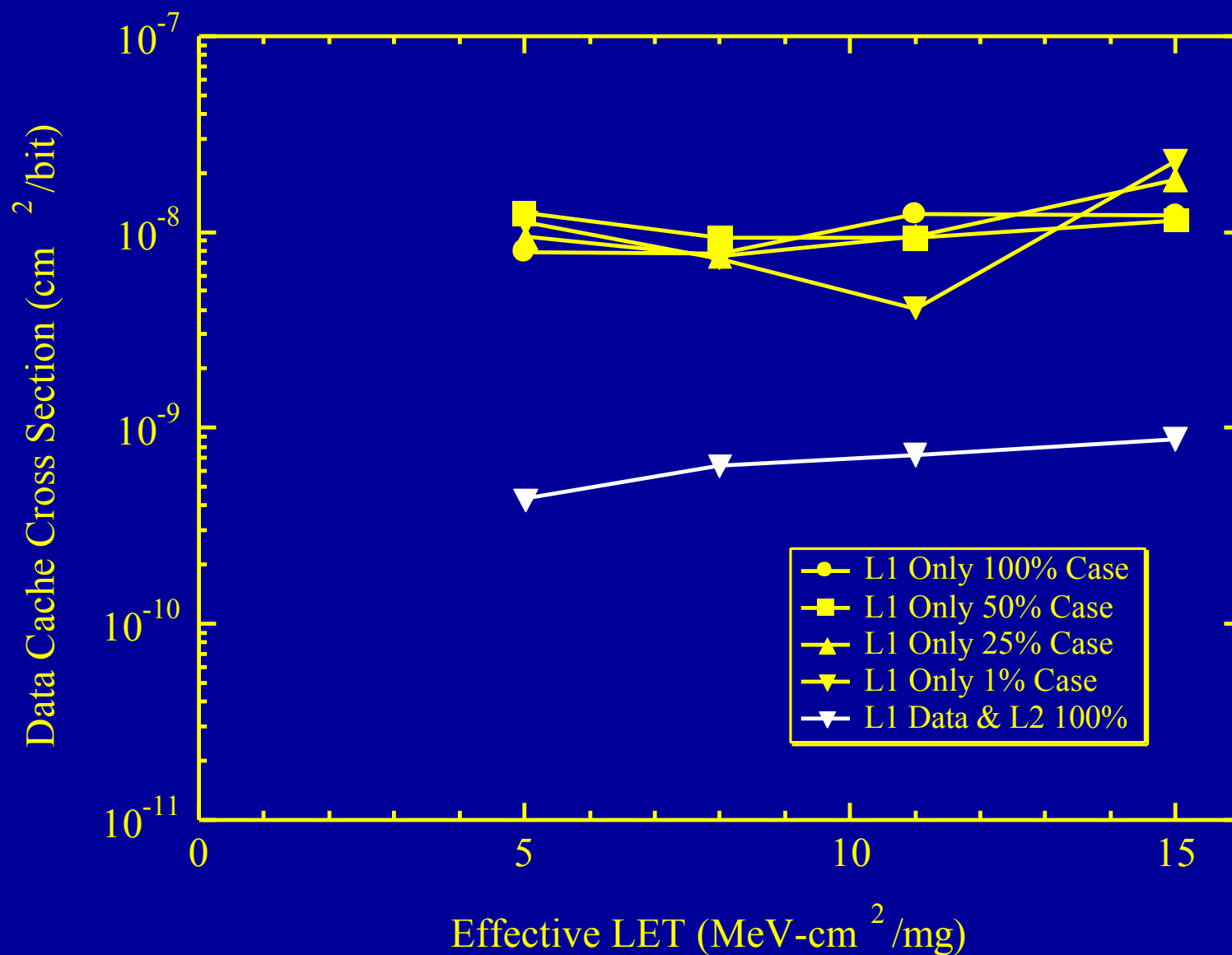| DUT	Test	Number of Upsets	Fluence (p/cm^2)	Cross Section (cm^2)	Cross Section Error
P3	A	5	2.39×10^{11}	3.93×10^{-11}	1.76×10^{-11}
P3	B	0	2.56×10^{11}	$< 9.59 \times 10^{-12}$	9.59×10^{-12}
P3	D	2	3.96×10^{11}	2.36×10^{-11}	1.67×10^{-11}
P3	F	2	3.92×10^{11}	2.02×10^{-11}	1.43×10^{-11}
P3	G	1	2.62×10^{11}	1.05×10^{-11}	1.05×10^{-11}

Proton Summary Data

Heavy Ion SEFI Data
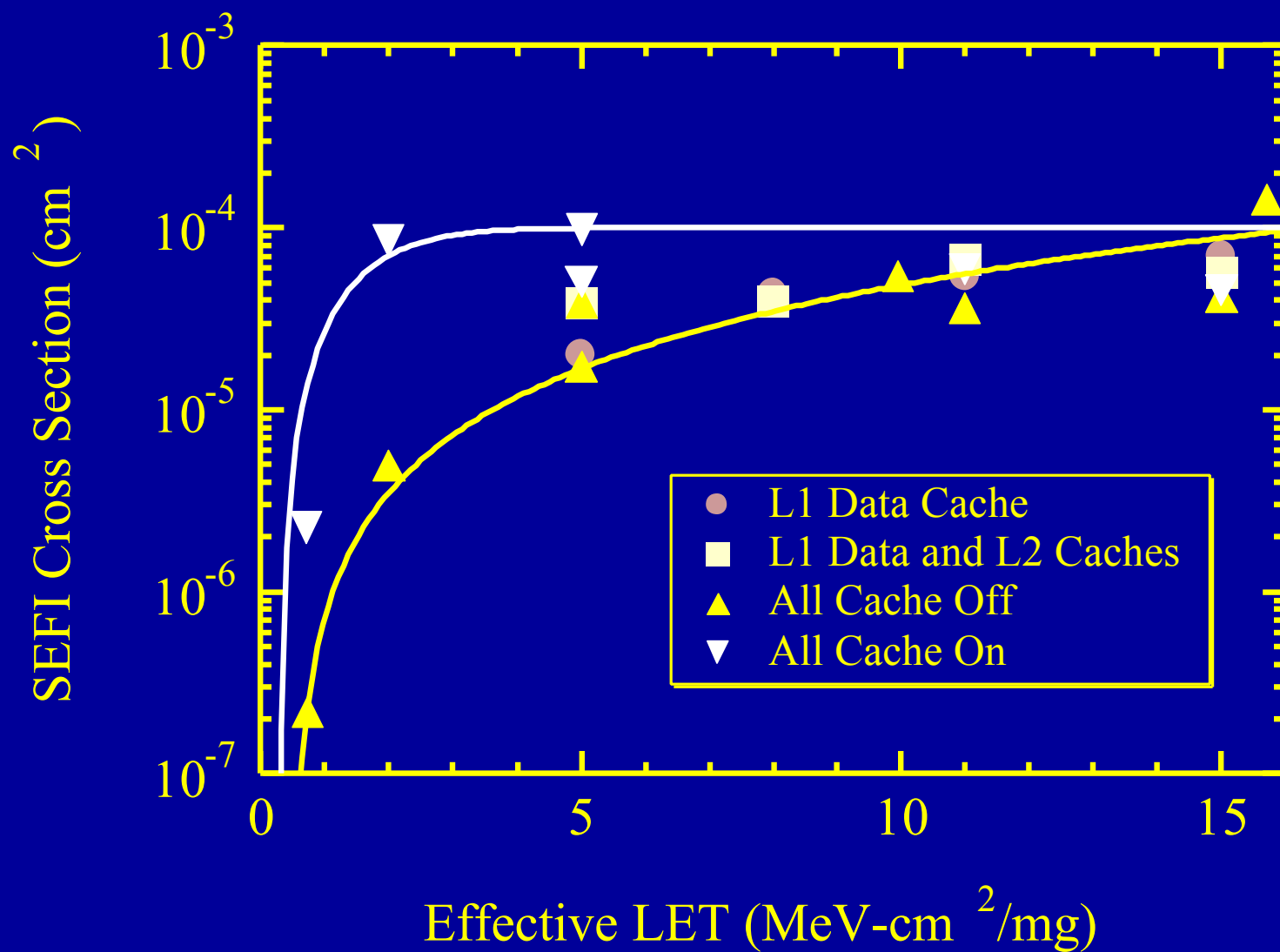
Heavy Ion SEE Data

Summary

- Extensive data has been collected on the total ionizing dose and single event response of the Intel Pentium III microprocessors.

- The data indicates:
  - high tolerance to TID
  - no susceptibility to SEL from protons or heavy ions to an LET of 15 MeV-cm^2/mg
  - Single event upsets and functional interrupts are present

- Care must be taken in testing parts like the P3 where it must be treated like a "black box". Our cache testing showed a dramatic difference in test results simply by how the cache is utilized.